Application Note

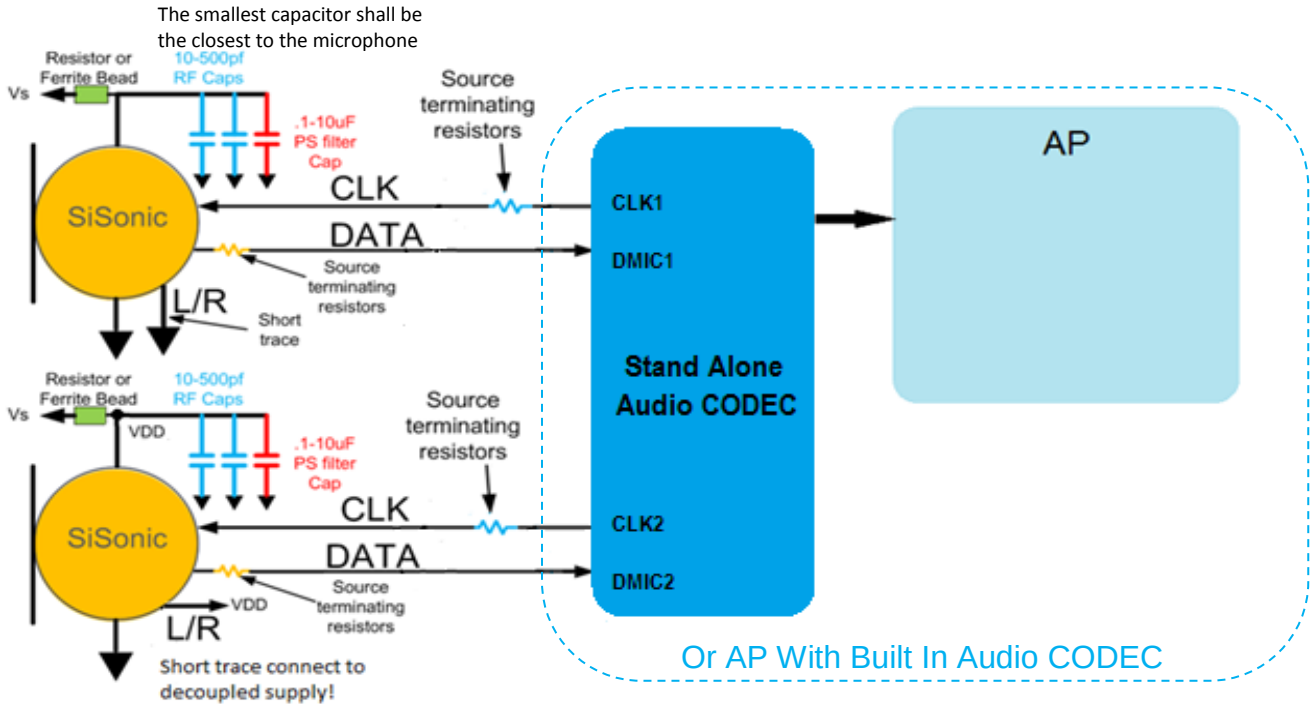
Multi-mode Digital SiSonic™ Microphone

Introduction

SPH0641LM4H-1 is the first multi-mode, sensitivity matched, high-performance, low power digital SiSonic™ microphone with a single bit PDM output in the market with extended wideband frequency response. This device is suitable for applications such as cell phones, smart phones, tablet, laptop computers, sensors, digital cameras, portable music recorders, and other portable electronic devices where excellent wideband audio and RF immunity are required.

The goal of this application note is to give customer a better understanding of how this new multi-mode digital SiSonic™ microphone works and how to properly implement it into their application.

Reference Circuit #1: Independent Microphone with Separate Clock Connections



***Note:** Allows independent mode control for each microphone if the CODEC can support independent clock rates.

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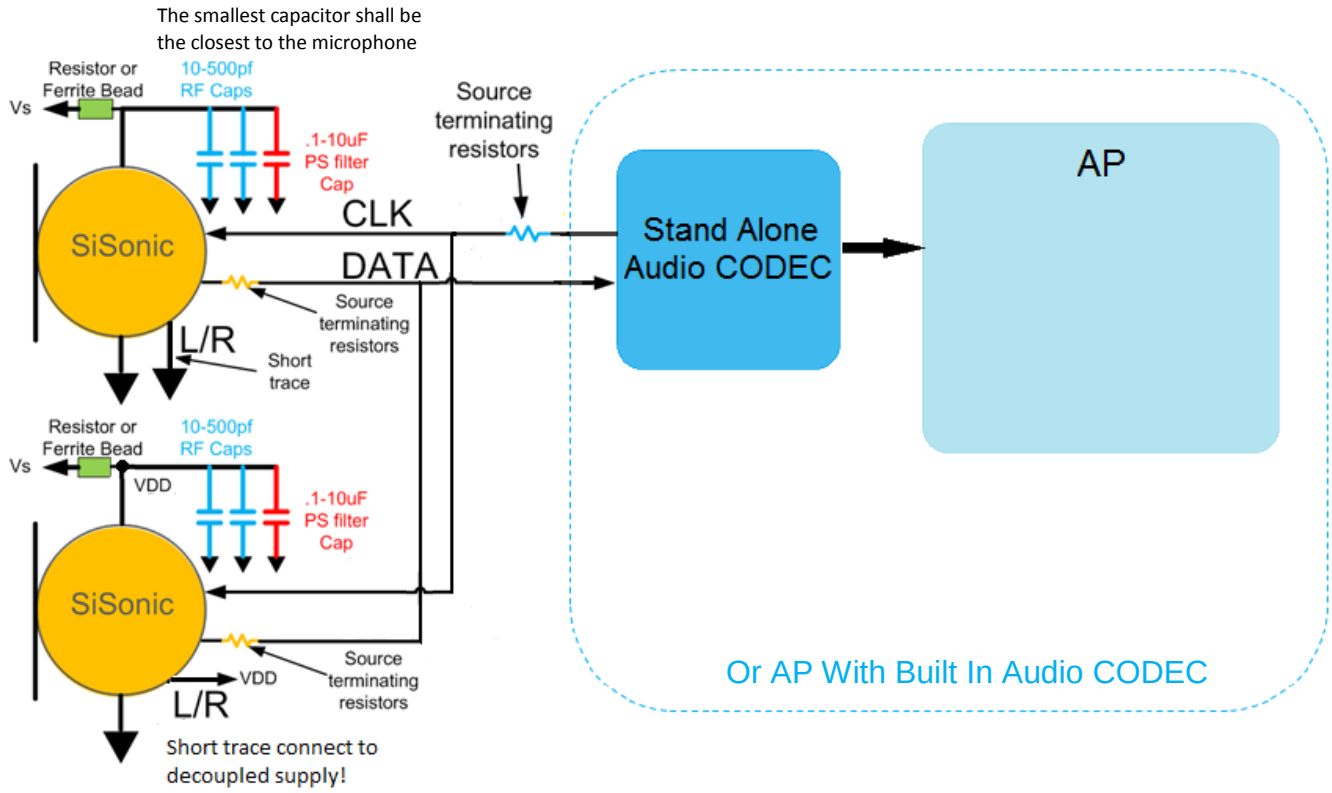
Reference Circuit #2: Common Clock Connection Diagram



***Note:** Both microphones have to be powered on and off simultaneously otherwise the data output of "ON" microphone will be pulled low by the "OFF" microphone.

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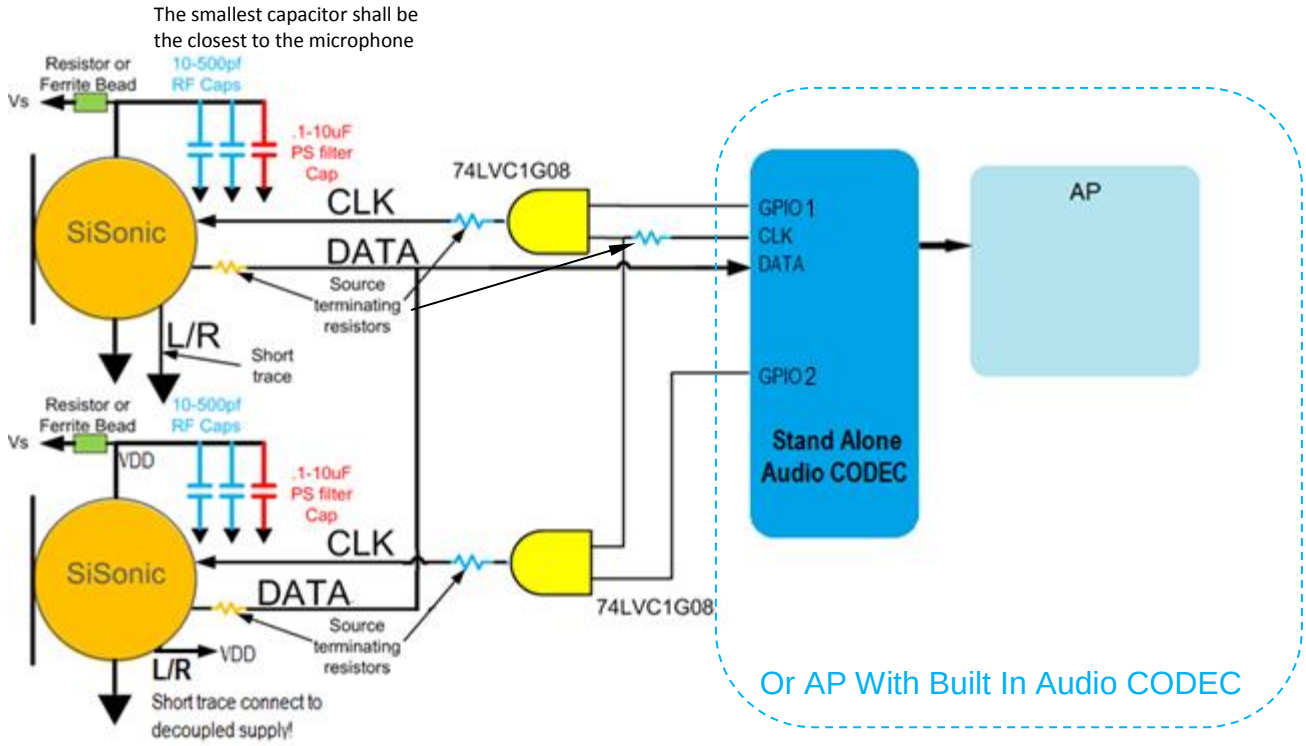
Reference Circuit #3: Common Clock With Independent Sleep Mode Control, VDD Always On



***Note:** Allows 2 microphones to share one data line while putting one microphone into sleep mode and the other in any one of the 3 modes or both in the same mode controlled by GPIO.

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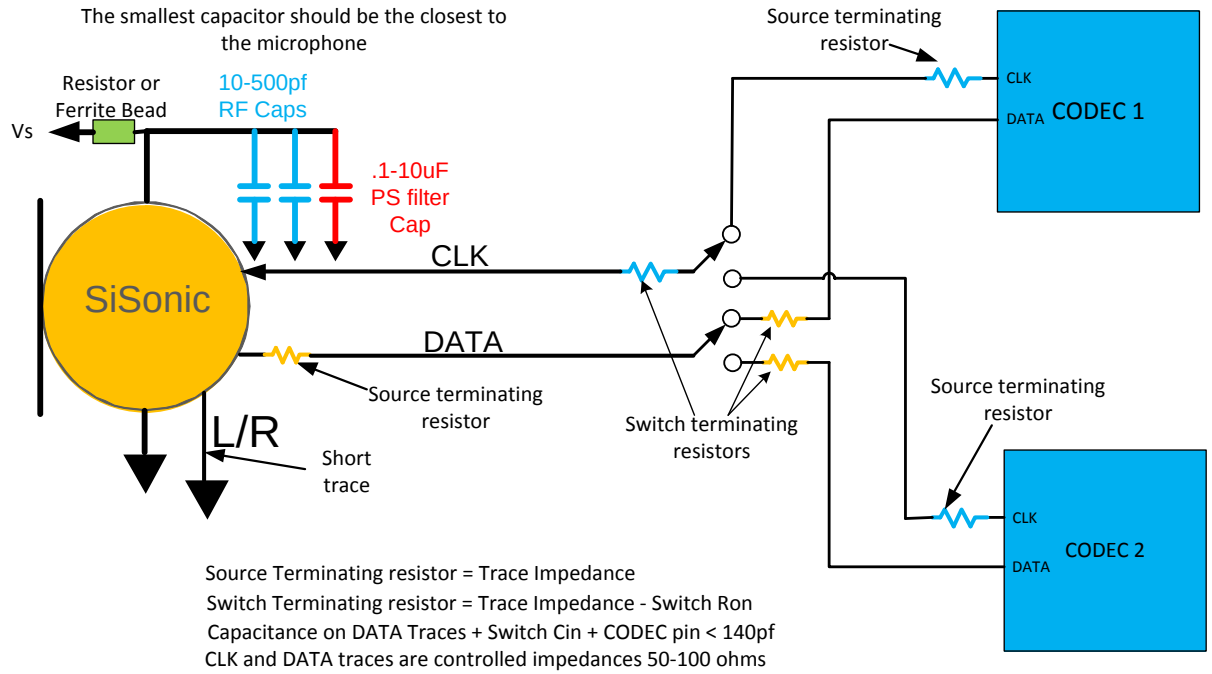
Reference Circuit #4: Common Microphone Switched Between Two CODECs, VDD Always On



Source Terminating resistor = Trace Impedance
Switch Terminating resistor = Trace Impedance - Switch Ron
Capacitance on DATA Traces + Switch Cin + CODEC pin < 140pf
CLK and DATA traces are controlled impedances 50-100 ohms

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Design At A Glance

- **Traces**
  - Use controlled impedance traces 50-100 Ohms for CLOCK and DATA lines.
  - Add source termination resistors close to the device driving the trace. Use the nearest 5% resistor value to match the impedance.
  - If a device is placed between the CODEC and microphone, add matching resistors after the device (see example circuits 3 and 4).
  - Keep the total capacitance of the DATA trace and connecting device to < 140pf
  - The microphone GND should be connected with a via to the ground plane, the via should be connected to the microphone GND pad without a trace

- **Decoupling**
  - Use NPO/COG ceramic capacitors.
  - Use 2 or 3 capacitors to cover wide band interfering frequencies. Match the resonant frequency of the capacitor to the interfering frequency.
  - Connect decoupling capacitors to VDD and GND with vias to the pad no trace
  - Use a series ferrite or resistor between the power supply and the decoupling capacitor(s).
  - The smallest value capacitor should be the closest to the microphone.

- **Board to Board Connectors**
  - There should be a ground pin next to each signal/power pin on board to board connectors to avoid increasing the inductance of the circuits passing through the connector.

***Note:** This list is NOT all inclusive, for further information, see High Speed Digital Design: A Handbook of Black Magic by Howard Johnson and Martin Graham.

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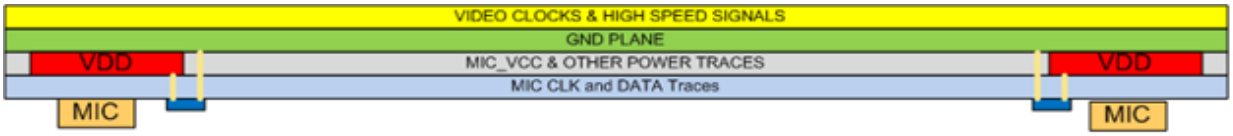
Decoupling Capacitor

In digital design, it is common practice to put a 0.1~10uF decoupling capacitor and several small value RF capacitors (10~500pF) close to the VDD pin of each digital microphone to provide microphone a clean stable bias. If the interfering signal frequencies are known, choose the capacitor so that it will resonate at the same frequency as the interfering signal. If there are other interferers, select capacitors that resonate at those frequencies.

Capacitors made with Class 2 dielectrics are not recommended to be placed near the microphone. These types of capacitors can generate acoustic noise due to their inherent piezoelectric effect.

Decoupling capacitors should connect directly to power planes through vias using minimal trace lengths. Put a small power plane under the microphone and use vias to connect the decoupling capacitors to the planes. Keep microphone CLK and DATA lines on the same layer away from other Hi-speed traces. Utilize the GND plane to shield between fast and slow signals.



Inductance in the connections of the decoupling capacitors reduces their effectiveness and can cause noise problems. The following shows different connection layouts and their respective inductances. **DO NOT** connect decoupling capacitors using leads (see “fat” and “skinny” trace inductances vs “side” and “end”) between the via and the mounting pad. **ALWAYS** connect the mounting pad directly to the via.

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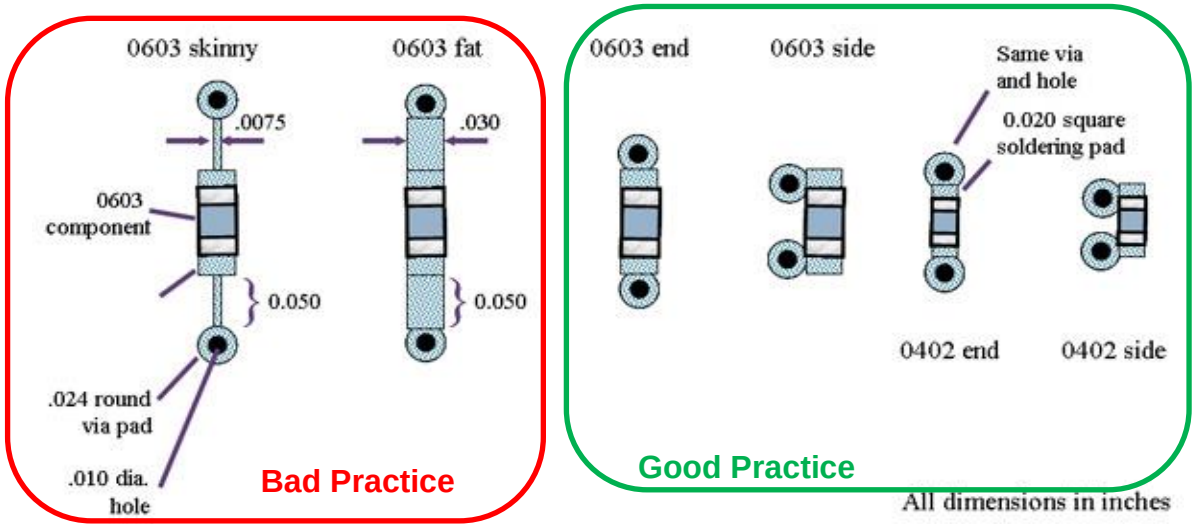

Table 1-Parasitic Inductance of Bypass Capacitors, nH, hole dia. 0.010 in.

Via length	0603 skinny	0603 fat	0603 end	0603 side	0402 end	0402 side
0.004	1.51	0.95	0.5	0.36	0.42	0.26
0.006	1.77	1.17	0.59	0. 46	0.5	0.32
0.01	2.18	1.52	0.77	0.61	0.67	0.4
0.02	2.87	2.23	1.16	0.85	1.01	0.6

Table 2-Parasitic Inductance of Bypass Capacitors, nH, hole dia. 0.020 in.

Via length	0603 skinny	0603 fat	0603 end	0603 side	0402 end	0402 side
0.004	1.51	0.89	0.42	0.33	0.38	0.21
0.006	1.66	1.12	0.53	0.38	0.44	0.25
0.01	2.13	1.47	0.68	0.51	0.58	0.32
0.02	2.68	2.07	1.07	0.67	0.82	0.43

Source Dr. Howard Johnson http://www.sigcon.com/Pubs/news/6_09.htm

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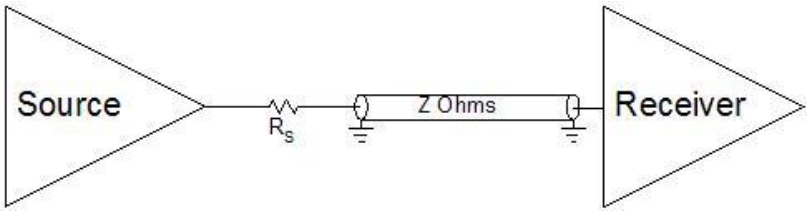
CLK and DATA Signal Routing

In high-speed digital systems, simple passive circuit elements like wires, cables, and chip PCB interconnections can significantly affect signal quality. High-speed digital edges contain frequency components that are several times the effective toggle rate of that signal. For example, a digital edge with a rise time of 1.5 ns contains significant amount of energy in frequencies up to 667 MHz, regardless of toggle rate. Any mismatching between the source and the receiver will cause reflections/ringing/overshoot/undershoot, which can result in incorrect signal reading or degradation of microphone performance. Severe overshoot/undershoot can lead to EMC problems.

Therefore, when routing CLK and DATA traces in order to avoid ringing and overshoot/undershoot, controlled impedance traces should be used. The schematic should be labeled to show the CLK and DATA traces are controlled impedances. Then the pc layout tool (assuming the correct stack-up parameters are set) will keep the trace impedance constant from layer to layer. A common practice to improve irregular CLK edges is source termination. Place a small series resistor close to the source and match the source impedance to the trace/transmission line impedance.



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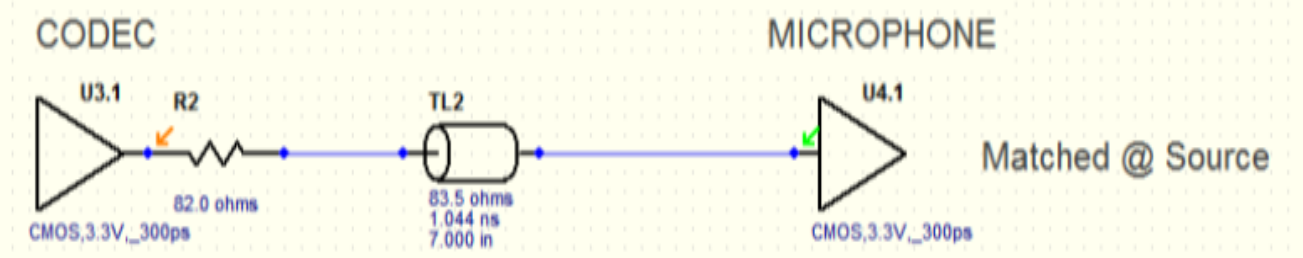
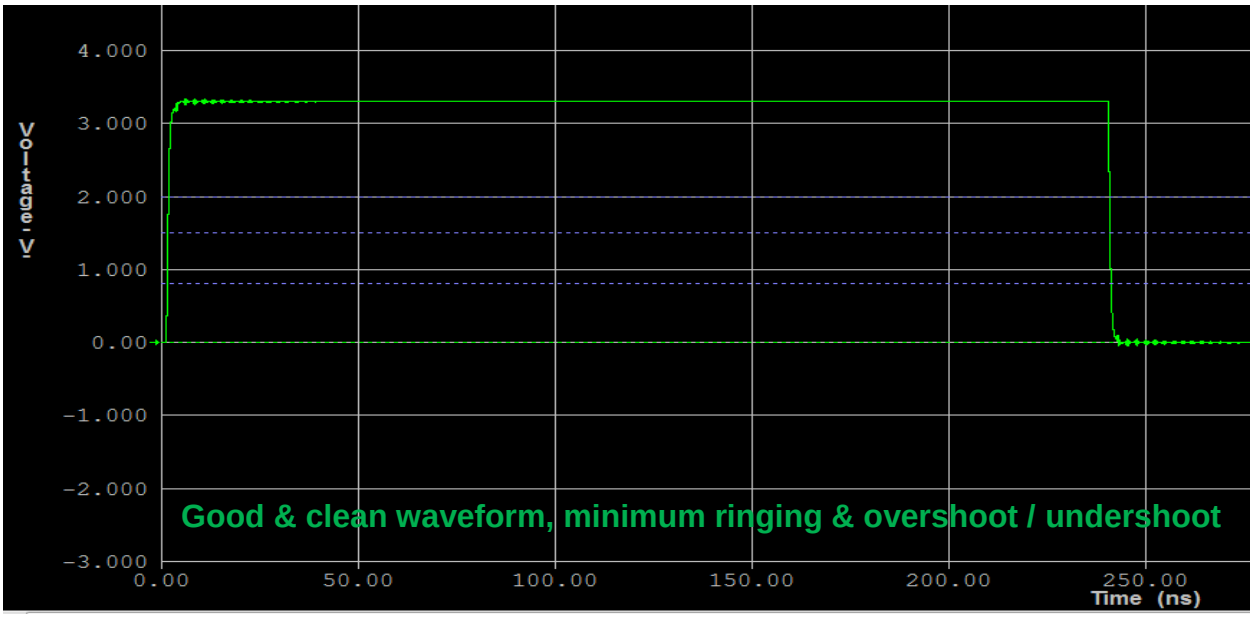
Here are some simulation results of different termination scenarios:

- **Impedance Match Series Resistor By The Source**





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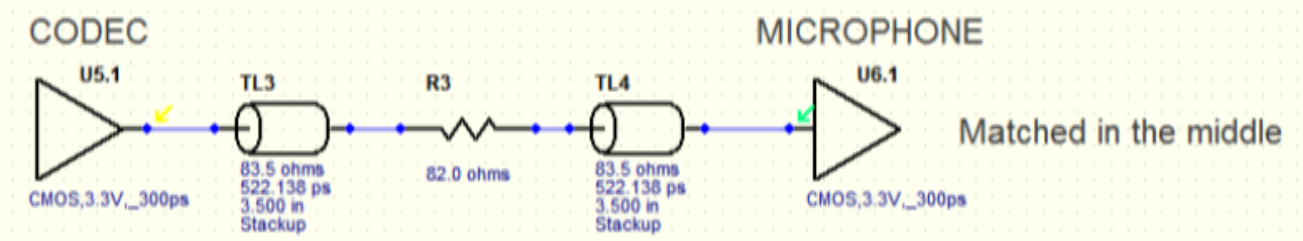
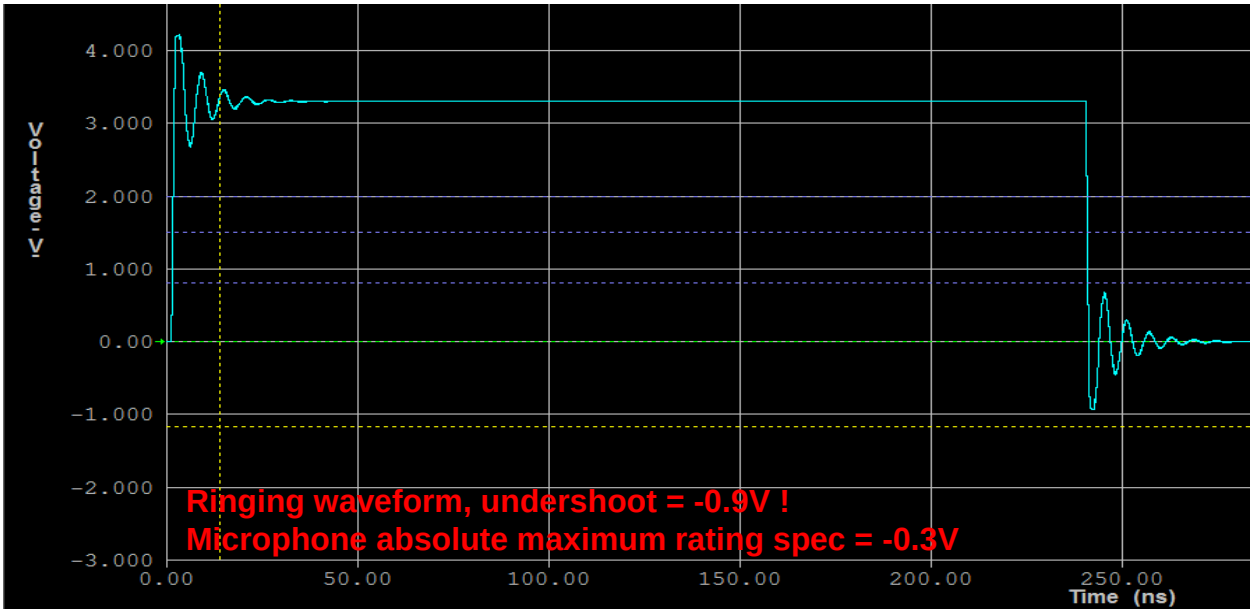
- **Impedance Match Series Resistor In The Middle**





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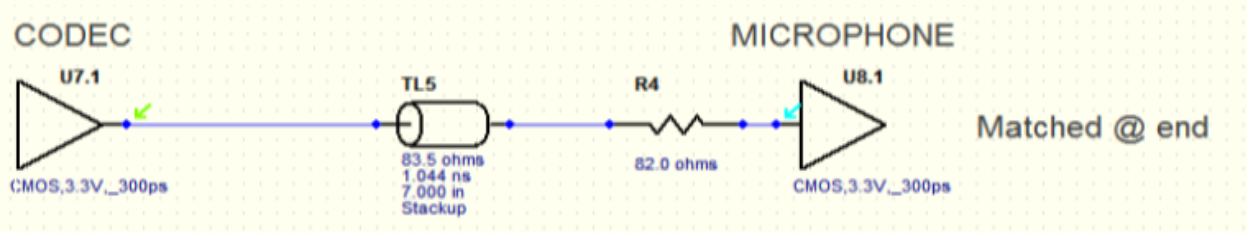
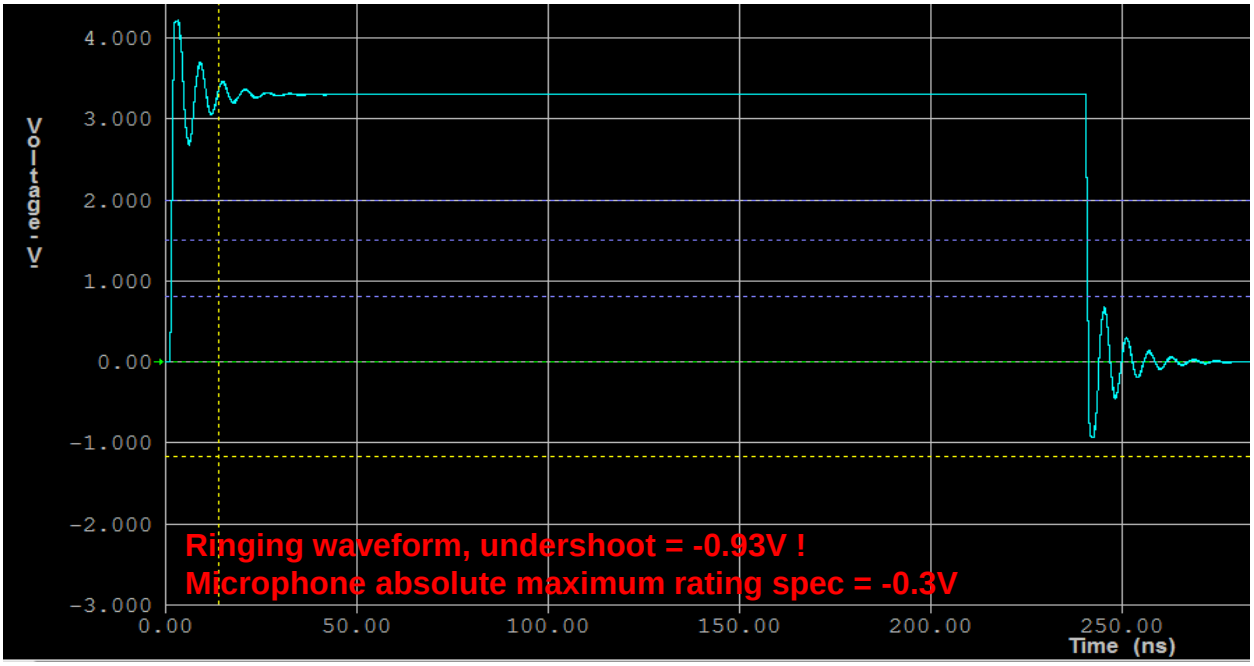
- **Impedance Match Series Resistor By the Receiver**





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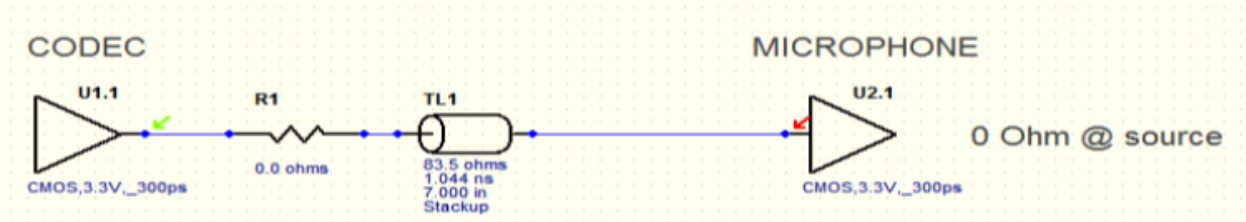
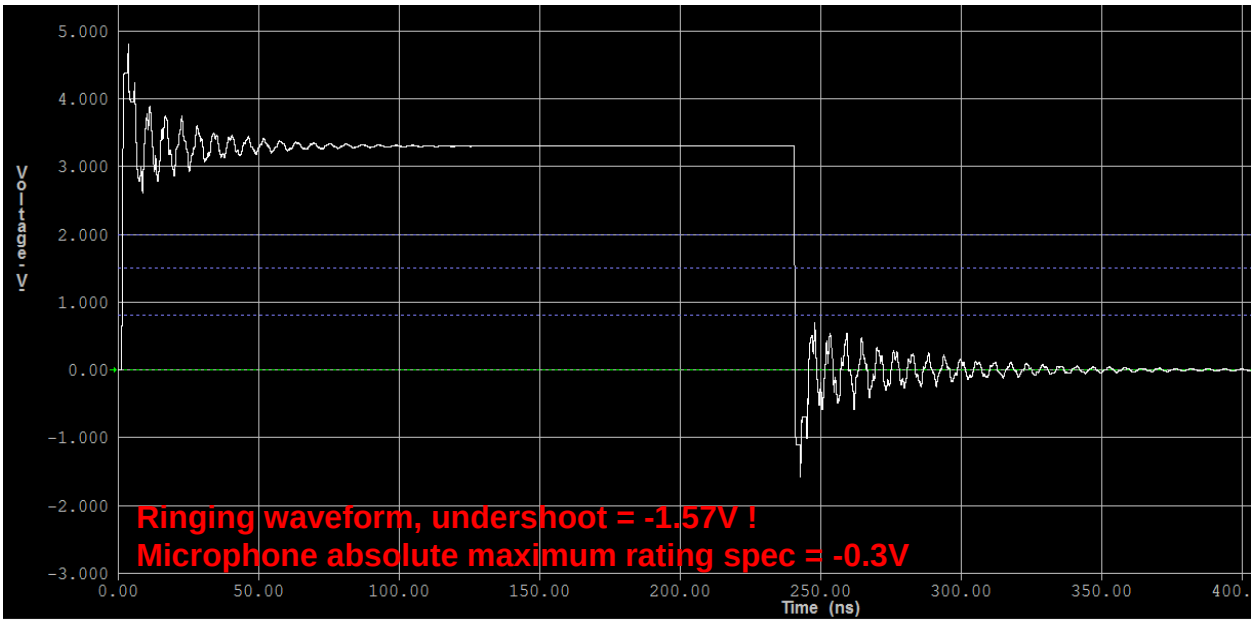
- **No Termination**





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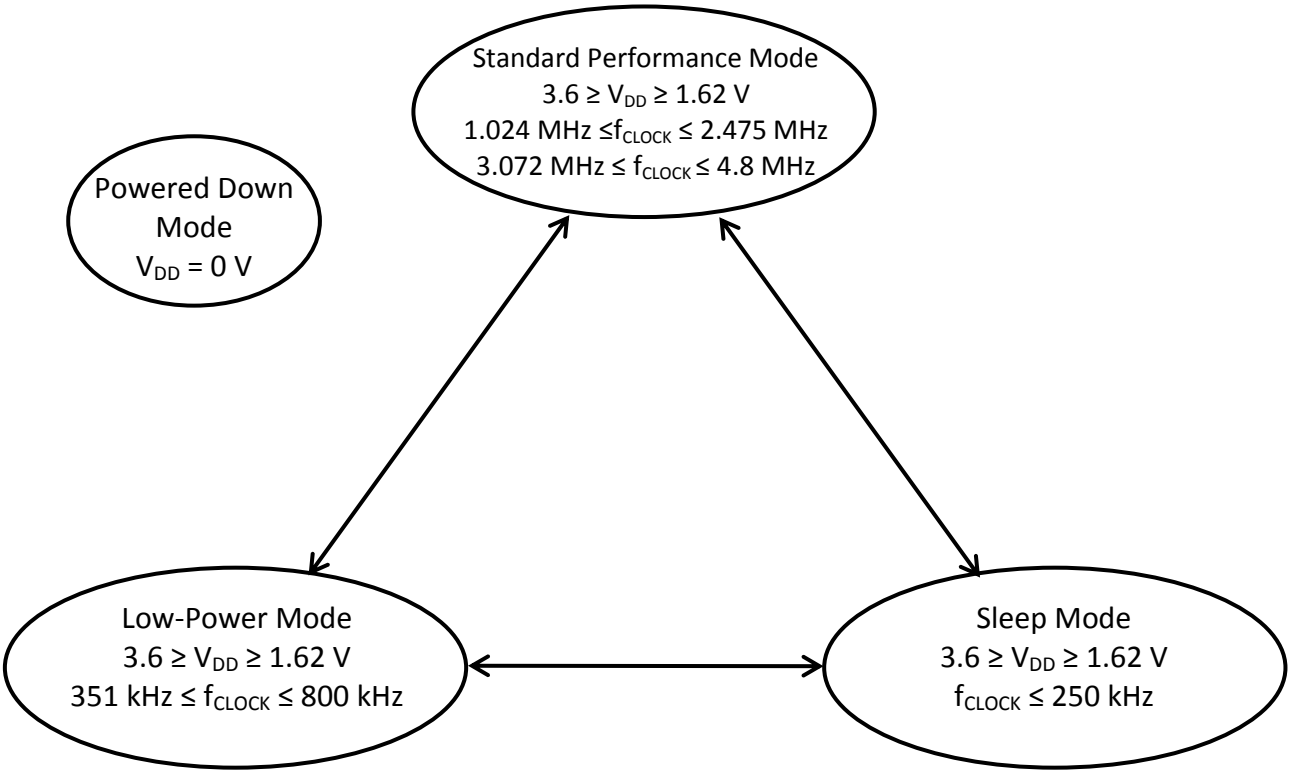
Multi-Mode
(Sleep Mode/Low-Power Mode/Standard Performance Mode)

Mode selection is controlled by the microphone's clock frequency. The system will need to be able to easily switch clock frequency to enter different microphone modes.

Here is the state diagram:



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The microphone is muted for 10ms during the mode changing to smooth the transient. An audible “Pop” sound may occur due to the mute. This can be easily handled or muted using application software.

Frequency Bandwidth

For a PDM system, the bandwidth of the output signal is depended on the clock frequency and digital decimation factor. Here’s the formula:

BW = $(f_{clk})/(2*\text{Decimation Factor})$, where f_{clk} = clock frequency. 64 is a typical factor for digital microphone decimation.

For example, multi-mode SiSonic™ digital microphones can achieve signal bandwidths of 768KHz/(2*48) = 8kHz in Low-Power Mode, and 2.4MHz/(2*64) = 18.75kHz or 3.072/(2*64) = 24KHz in Standard Performance Mode by varying the clock frequency and digital decimation factor.

The system/CODEC may need to be able to support different clock frequencies and decimation factors for different applications.

Current

For digital systems, the total current consumption is heavily dependent on the system capacitance loads, VDD levels and clock frequencies. For digital microphones, IDD varies with C_{LOAD} according to:

$\Delta I_{DD} = 0.5*V_{DD}*\Delta C_{LOAD}*f_{CLOCK}$.

Here are some measurement data to help illustrate the effects of microphone bias, system capacitance load and clock (frequency, logic level, slew rate) on microphone current consumption:

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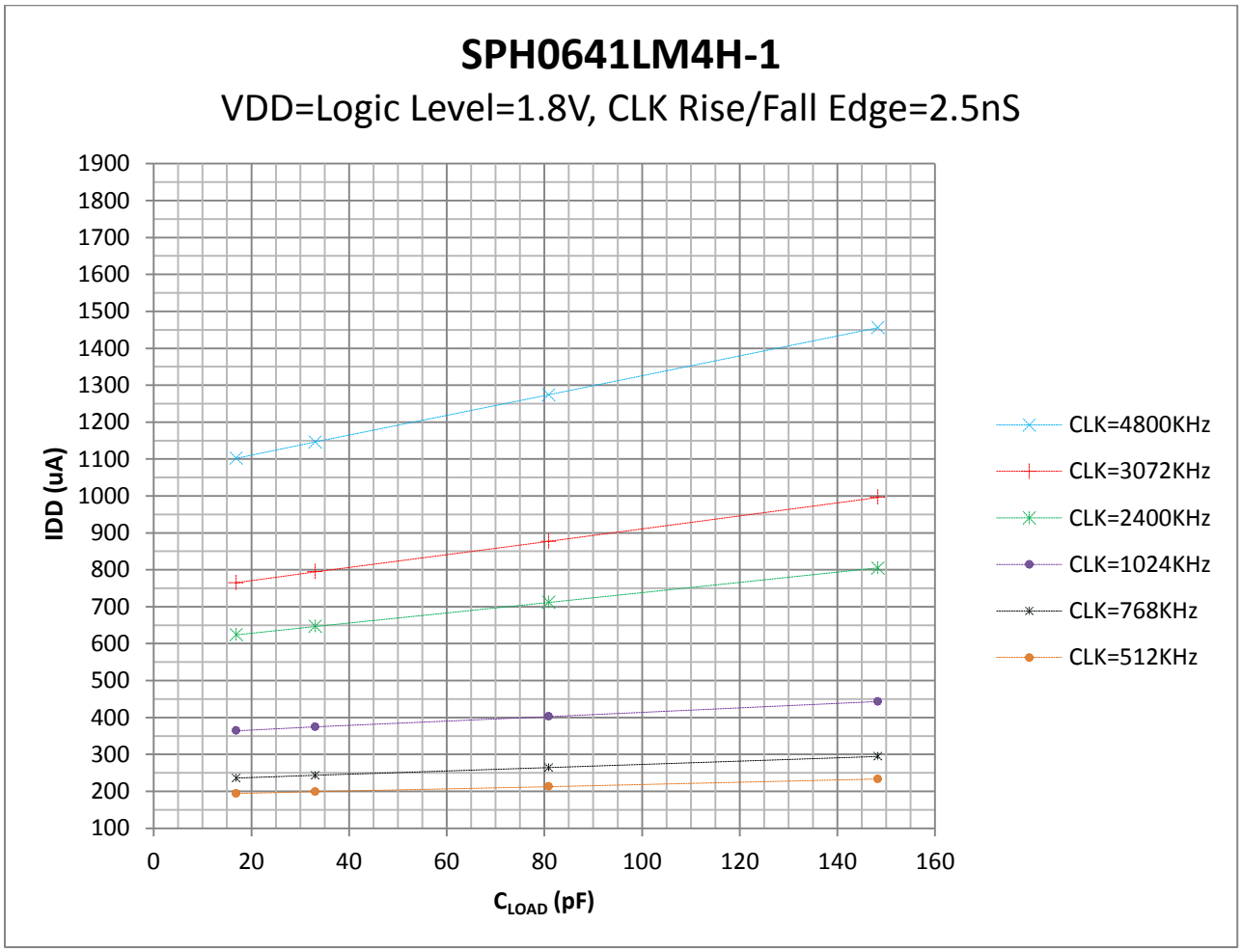
- **IDD VS C_{LOAD} VS CLK Frequency**



IDD VS C_{LOAD} VS CLK Frequency at 1.8V Mic Bias

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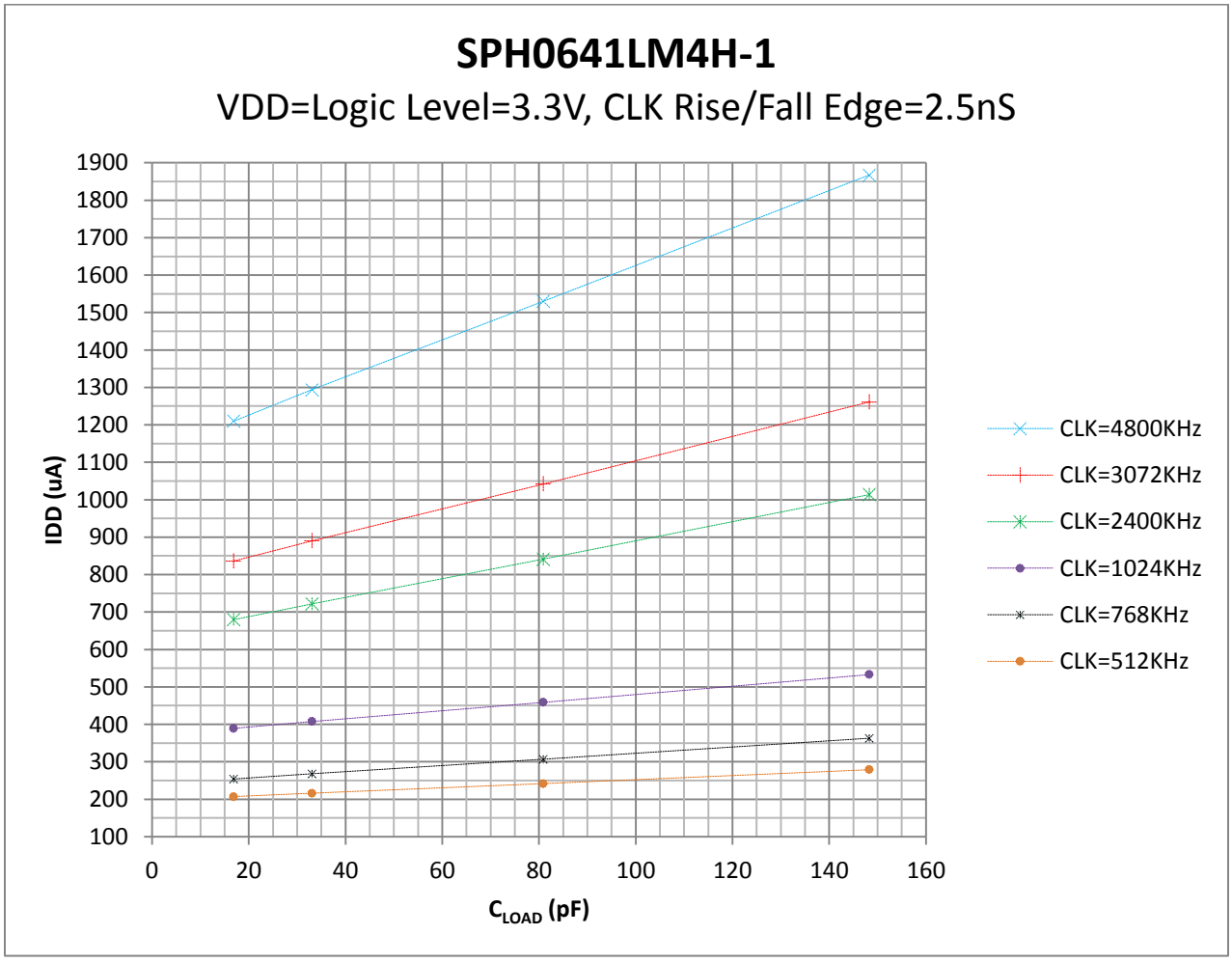

IDD VS C_{LOAD} VS CLK Frequency at 3.3V Mic Bias

The capacitance of a typical BNC cable is around 30pf/ft. To save more current, minimize system capacitance load at microphone output and consider running the microphone at a lower clock frequency & VDD level.

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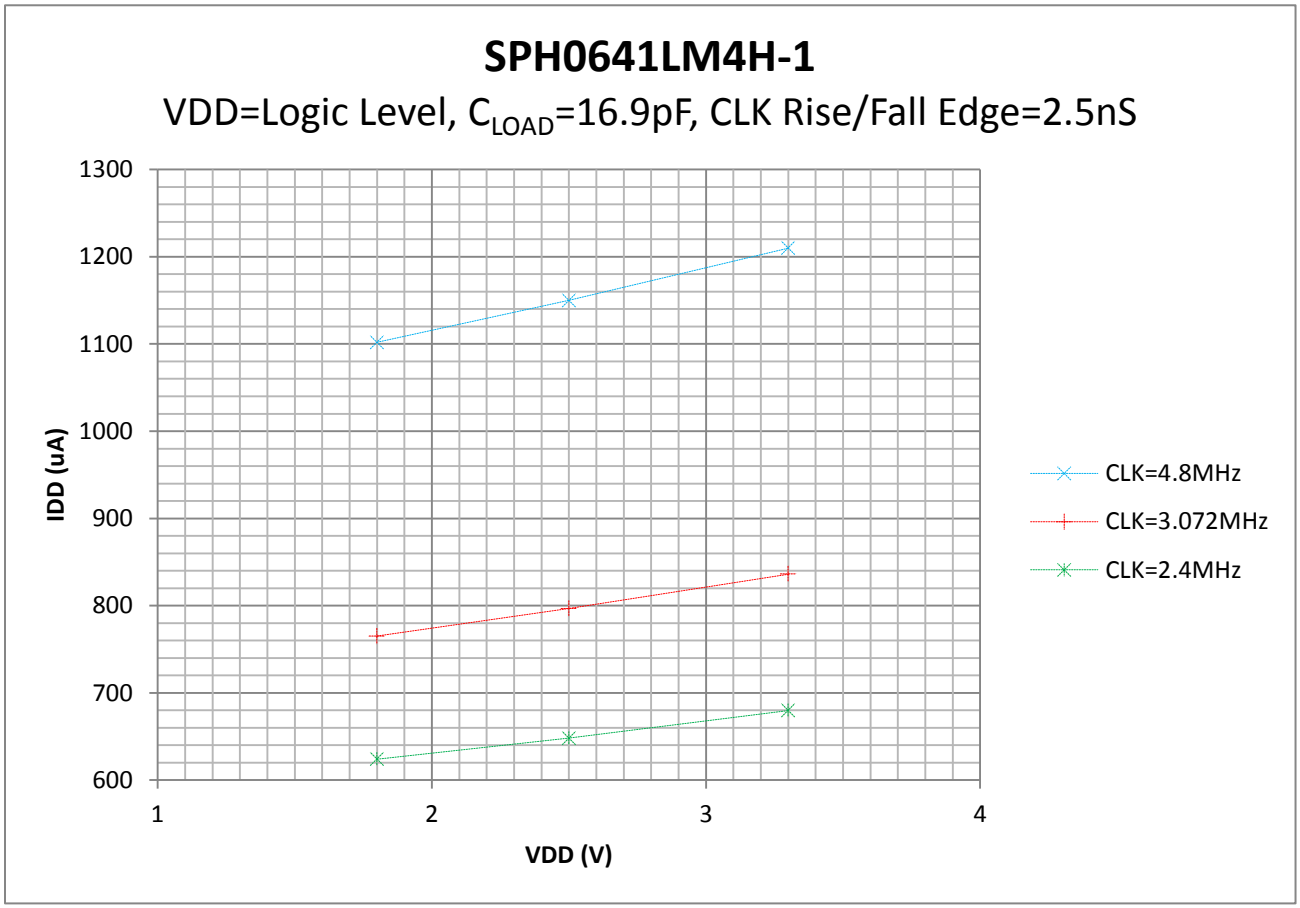
- **IDD VS VDD VS CLK Frequency**

Lower the system operating voltage levels always a good way to save power.



IDD VS VDD VS CLK Frequency with 16.9pF load

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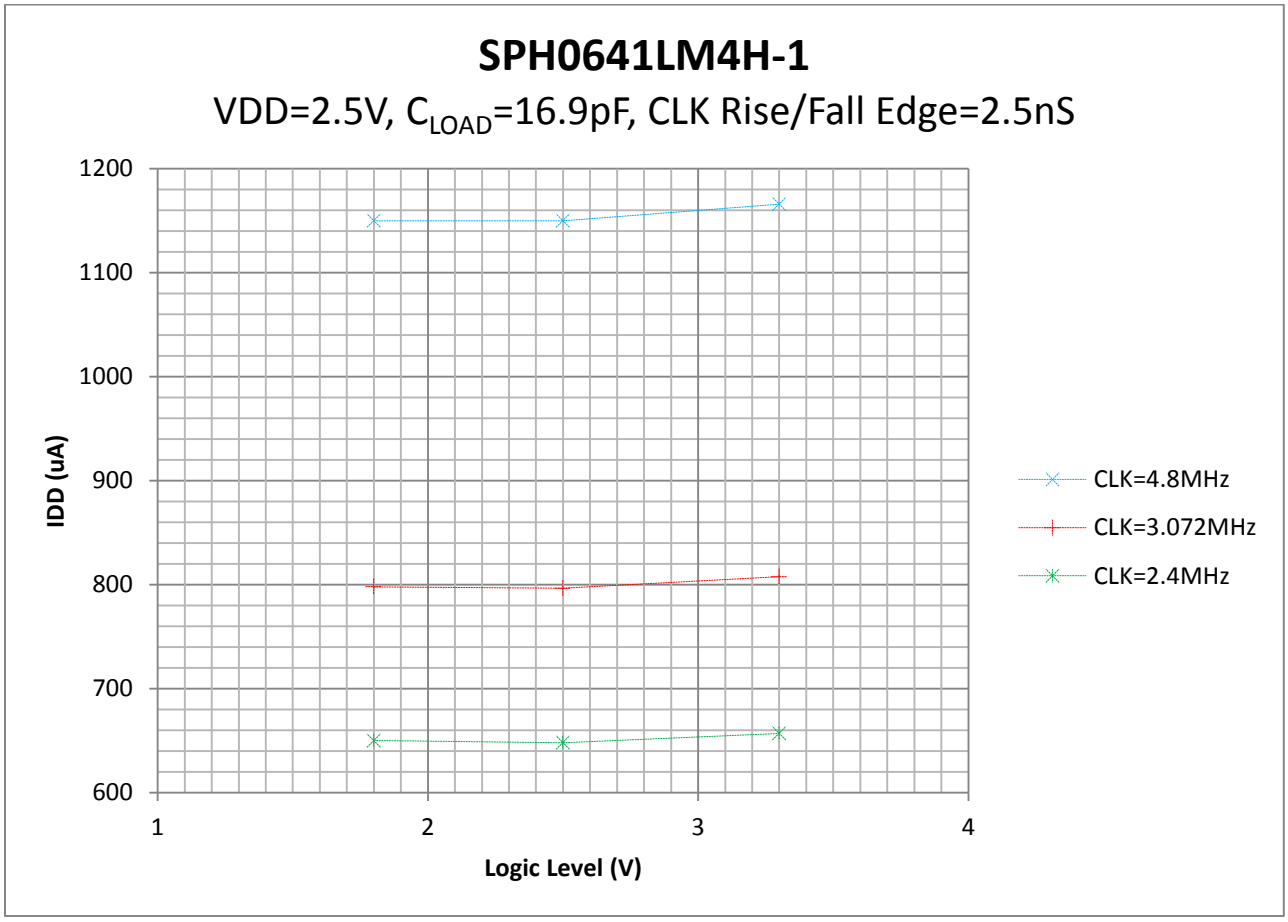
- **IDD VS Logic level VS CLK Frequency**

Difference between microphone bias and clock logic level will slightly increase microphone current draw.



IDD VS Logic level VS CLK Frequency at 2.5V mic bias with 16.9pF load

***Note:** For digital system, system logic level needs to be compatible with microphone logic level (which is relative to microphone bias level).

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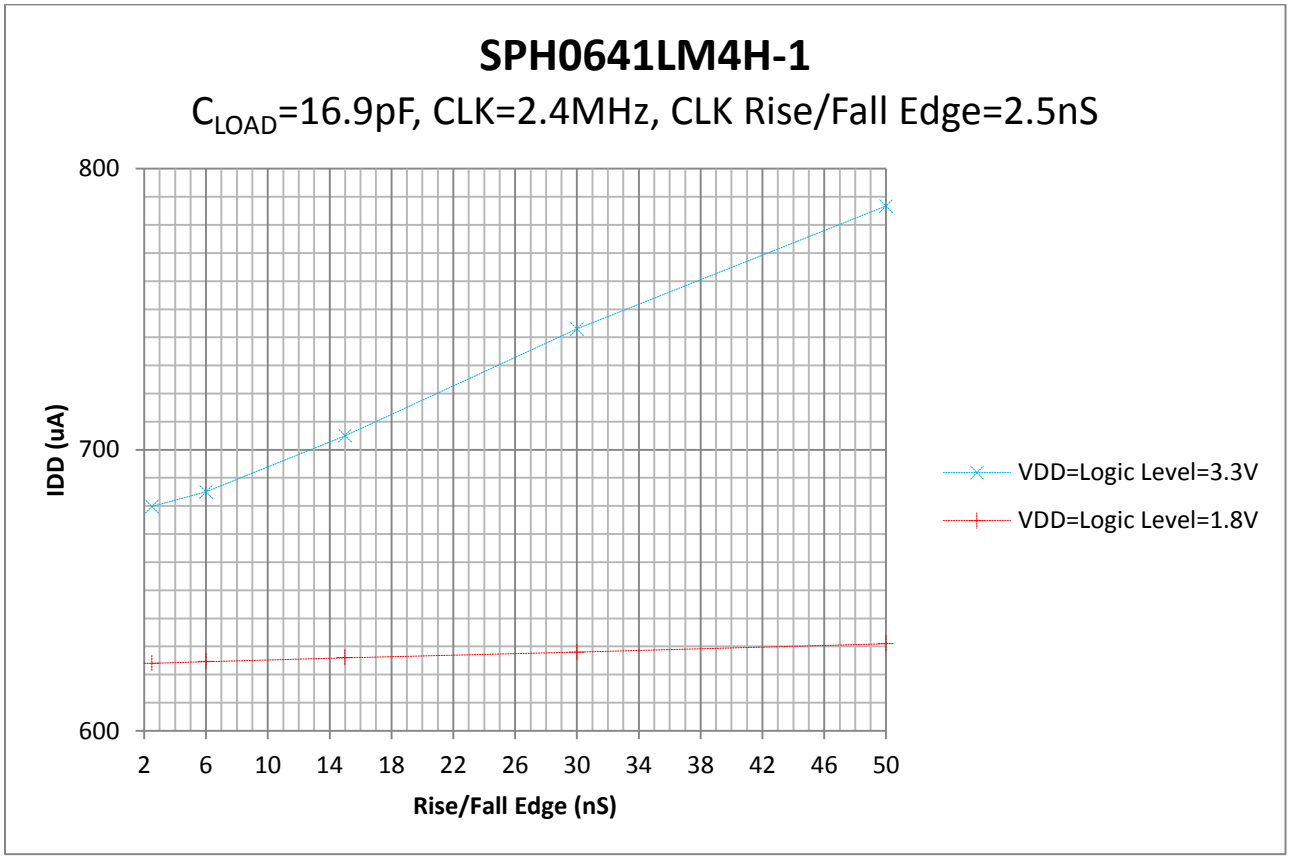
- **IDD VS CLK Rise/Fall Edge VS VDD**

Slower the clock slew rate will increase microphone's current draw.



IDD VS CLK Rise/Fall Edge VS VDD at 2.4MHz with 16.9pF load

***Note:** The clock rise/fall time (30%/70%) is 3ns max. in the data sheet.

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